SerDes 系統簡介
及相關數位訊號處理技巧

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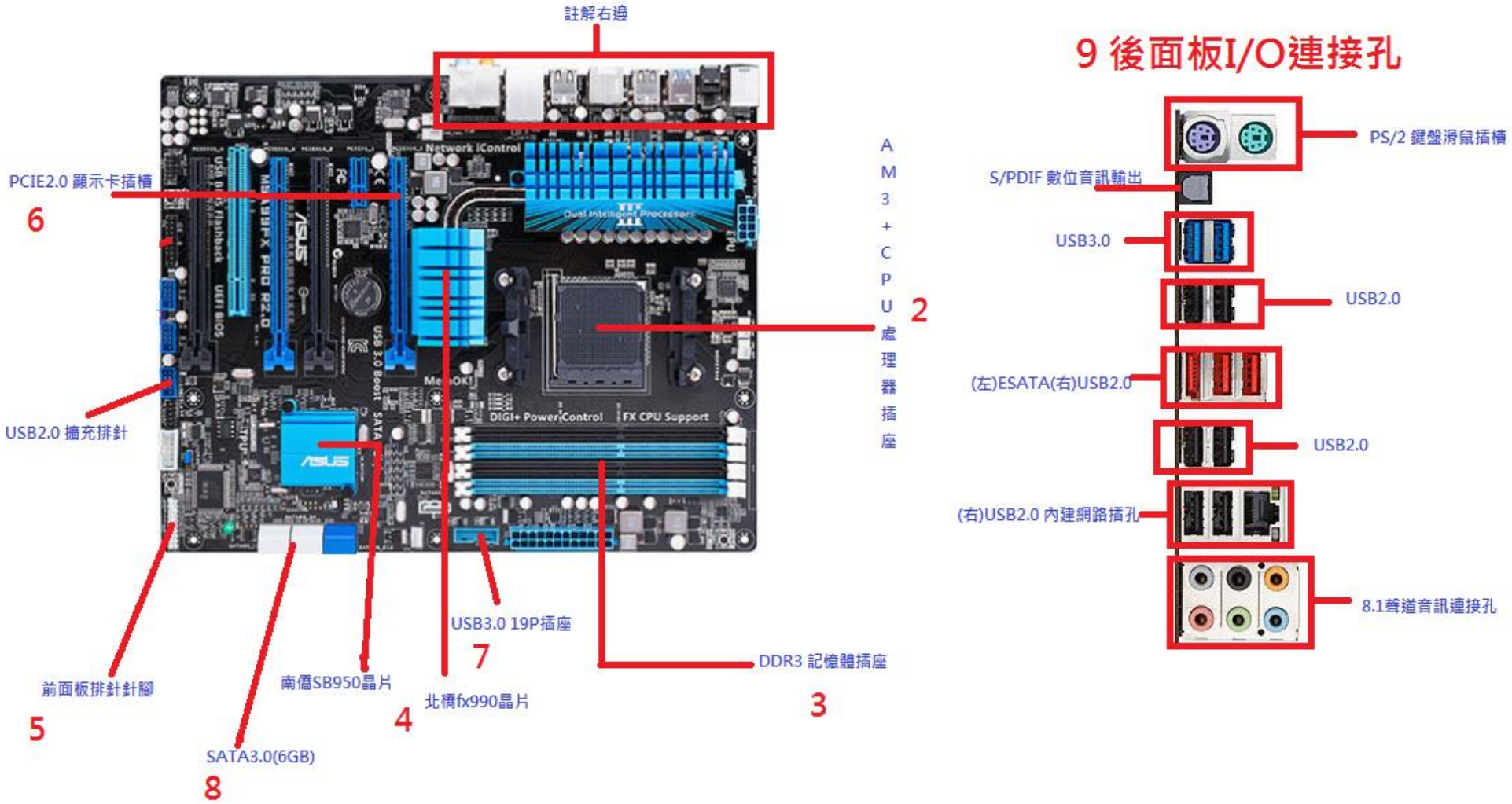
Outline

- Introduction
- Parallel & Serial Interface
- SerDes 簡介
- Line Coding
- DC & AC coupling
- 8b/10b encoding
- SerDes 電路介紹
- 總結

電腦主機板

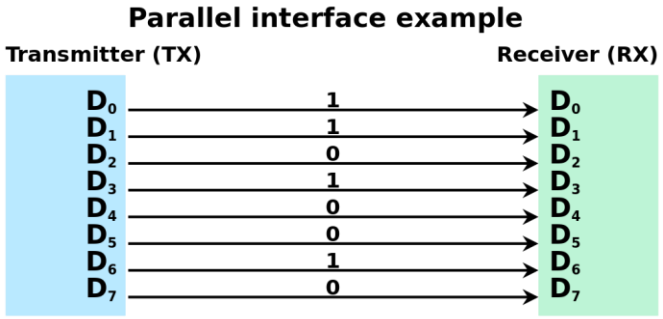


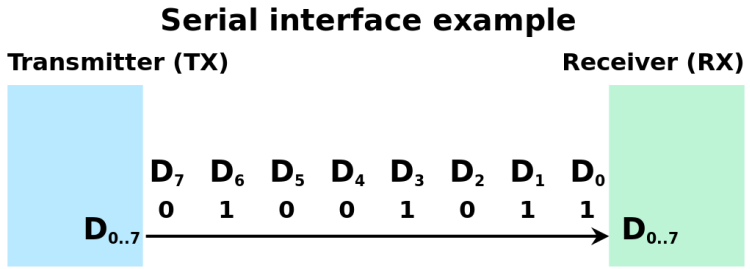
圖片來自asus官網主機板型號: AMD AM3+ M5A99FX PRO 2.0

匯流排（Bus）

- 電腦組件間規格化的資料交換方式
- PC上一般有五種匯流排：
  - 資料匯流排（Data Bus）：在CPU與RAM之間來回傳送需要處理或是需要儲存的資料。
  - 位址匯流排（Address Bus）：用來指定在RAM（Random Access Memory）之中儲存的資料的位址。
  - 控制匯流排（Control Bus）：將微處理器控制單元（Control Unit）的訊號，傳送到周邊裝置
  - 擴充匯流排（Expansion Bus）：可連接擴充槽和電腦。
  - 局部匯流排（Local Bus）：取代更高速資料傳輸的擴充匯流排。
- 匯流排頻寬（單位時間可傳輸資料量）= 頻率×寬度（Bytes/sec）

Parallel v.s. Serial Interface

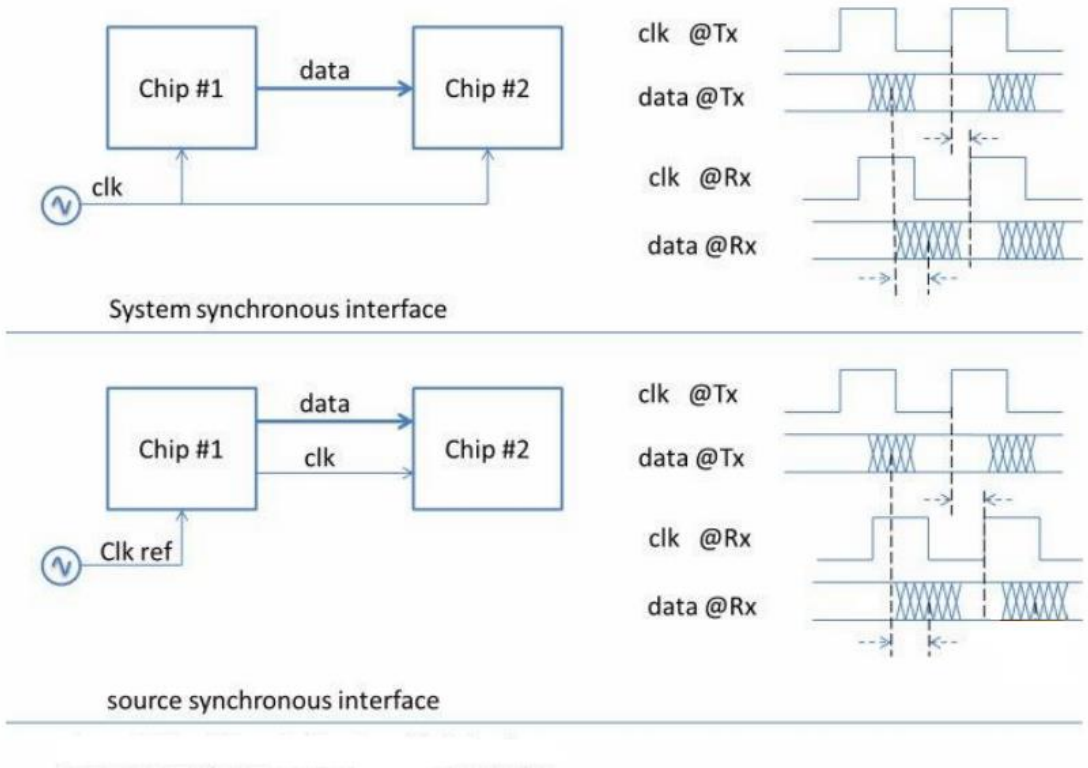




Parallel: Multiple connections between chips	Serial: Single connection pair
Power consumption ↑	Power consumption↓
Complex packages, bigger IC	Fewer pins, compact IC
Susceptible to EM interference	Robust EM performance
Challenging skew balancing requirements	Clock can be recovered from data
Lower latency	Higher latency
DDR	SerDes

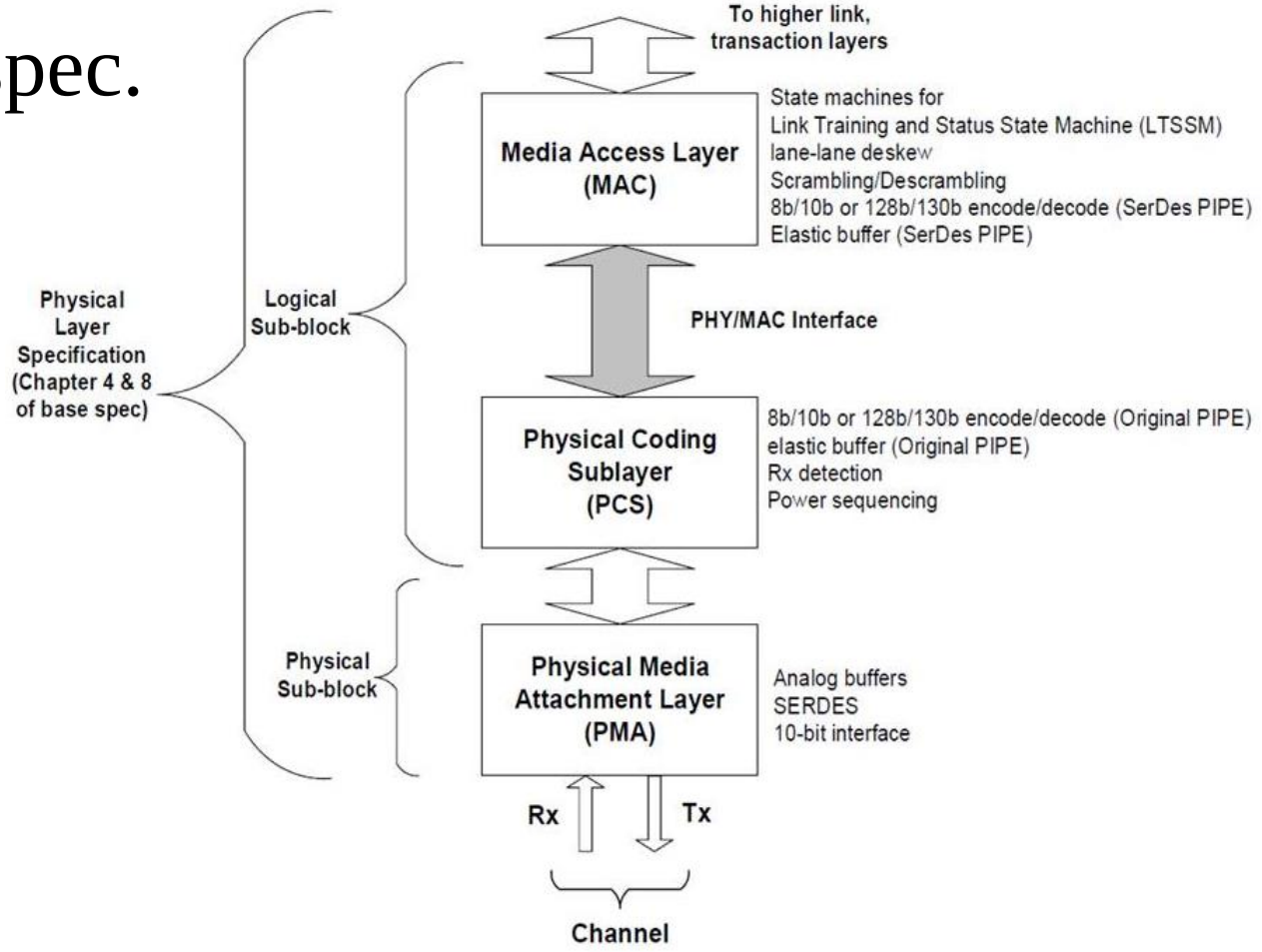
數位訊號傳輸

- 需要定義Clock
- **Source Synchronous:**
  - 一條線送data，一條線送clock
  - 開始發送的時間要同步
  - 走線長度匹配，受RC delay影響
- **System Synchronous:**
  - 從data還原時間訊號

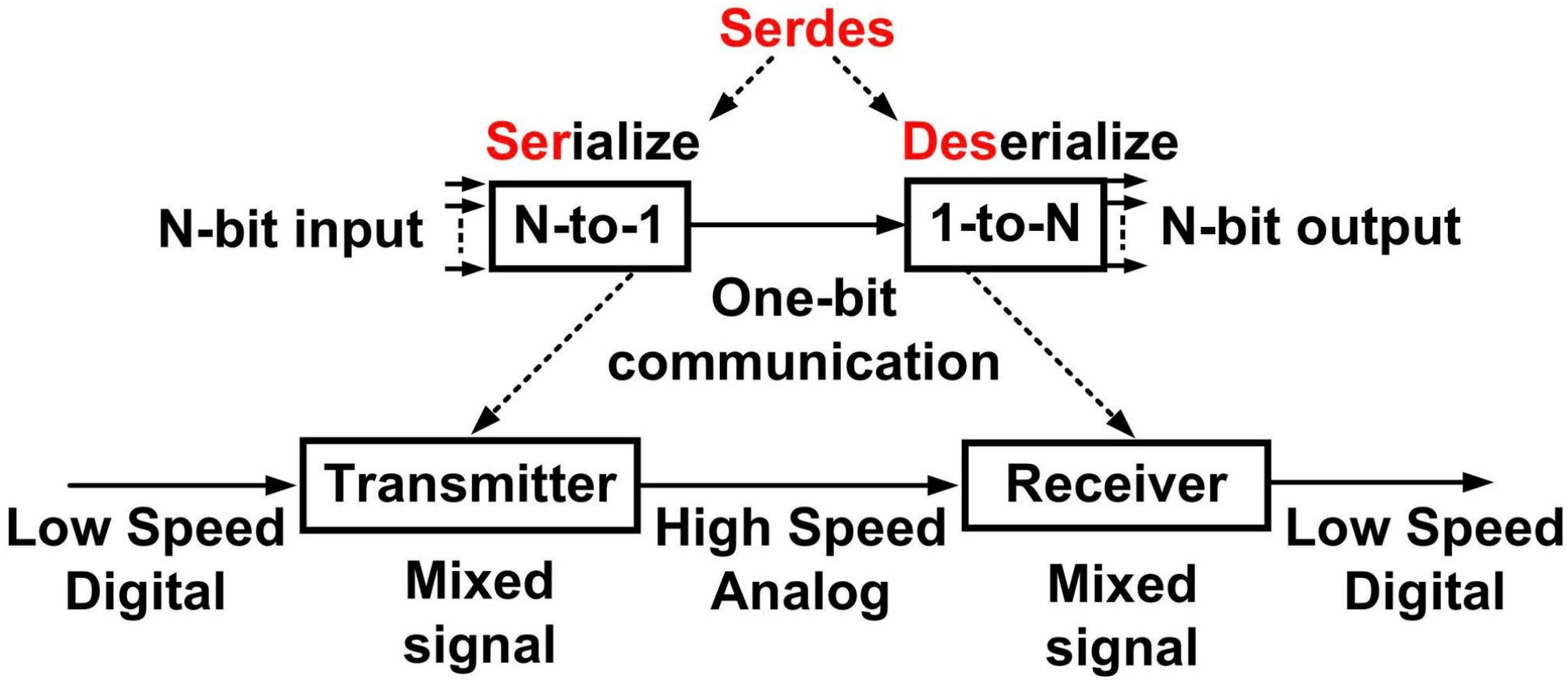


傳輸介面架構

- Protocal layer: Rule of communication
  - Encoding, procedure, etc.
- Physical layer: Electrical spec.
  - Eye mask, jitter tolerance, etc.



什麼是 SerDes?


Serdes
Serialize
Deserialize
N-bit input
N-to-1
1-to-N
N-bit output
One-bit
communication
Transmitter
Receiver
Low Speed
Digital
Mixed
signal
High Speed
Analog
Mixed
signal
Low Speed
Digital

SerDes 優點

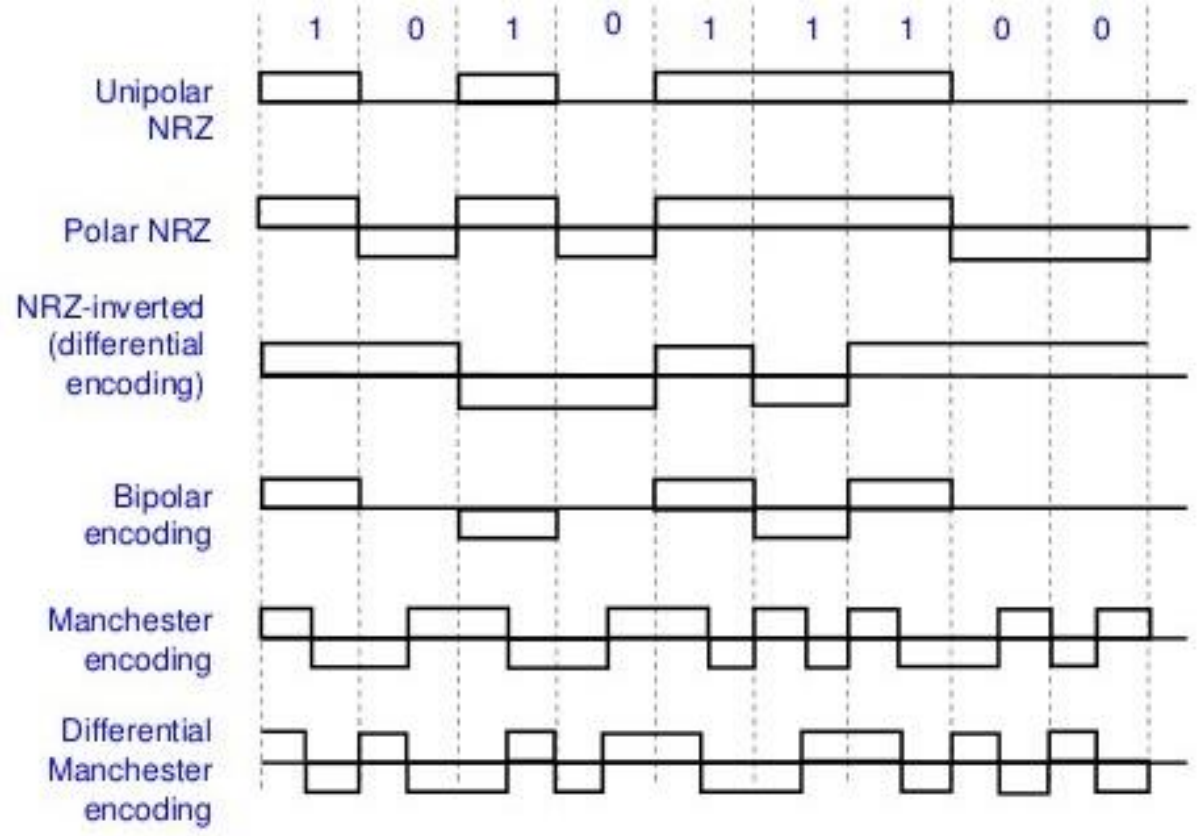
- 可在資料線中內嵌clock訊號，不需要額外傳送
- 透過Pre-emphasis/De-emphasis與Equalization技巧，可以實現高速長距離傳輸
- 使用較少引腳

Line Coding

- Unipolar Encoding
- Polar Encoding
- Bipolar Encoding
- Manchester Encoding
- Differential Manchester Encoding

Line Coding Examples

NRZ: Non Return to Zero



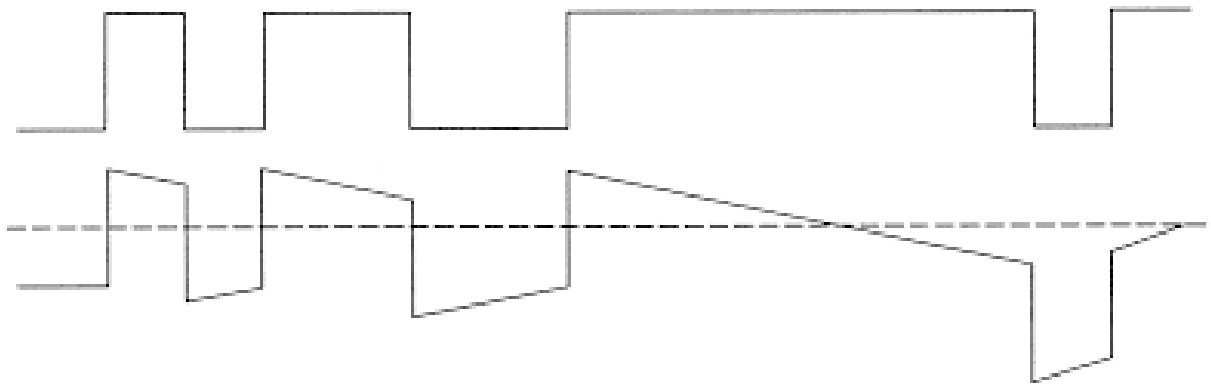
電路中常見
1:VDD
0:GND

AC & DC Coupling

- **DC coupling (Direct coupling):**
  - 訊號包含AC及DC成分
  - DC成分較不會受到導線RC low-pass影響，失真較低
  - 頻寬較大
  - High-definition video, e.g. HDMI.
- **AC coupling:**
  - Tx 端串聯電容，high-pass效果濾掉低頻成分
  - 消除DC offset
  - 兼容性: Tx/Rx可以給不同voltage level
  - 高速傳輸介面

DC balance

- 盡量傳送接近數量的「1」或「0」
- 定義連續「1」或「0」的可容忍最大值



8b/10b encoding

- 1983年由IBM的 Al Widmer 與 Peter Franaszek 所提出，用在光纖技術

- 至少在20位元「1」的個數與「0」的個數的差距不超過2個
- 沒有連續的5個「1」或「0」
- 8個位元→對映機制→ 10個位元的字碼

+2	+0	-2
4個「0」，6個「1」	5個「0」，5個「1」	6個「0」，4個「1」

資料碼

5b/6b [編輯]

5B/6B code

input		RD = −1	RD = +1	input		RD = −1	RD = +1
	EDCBA	abcdei			EDCBA	abcdei	
D.00	00000	100111	011000	D.16	10000	011011	100100
D.01	00001	011101	100010	D.17	10001	100011	
D.02	00010	101101	010010	D.18	10010	010011	
D.03	00011	110001		D.19	10011	110010	
D.04	00100	110101	001010	D.20	10100	001011	
D.05	00101	101001		D.21	10101	101010	
D.06	00110	011001		D.22	10110	011010	
D.07	00111	111000	000111	D.23 †	10111	111010	000101
D.08	01000	111001	000110	D.24	11000	110011	001100
D.09	01001	100101		D.25	11001	100110	
D.10	01010	010101		D.26	11010	010110	
D.11	01011	110100		D.27 †	11011	110110	001001
D.12	01100	001101		D.28	11100	001110	
D.13	01101	101100		D.29 †	11101	101110	010001
D.14	01110	011100		D.30 †	11110	011110	100001
D.15	01111	010111	101000	D.31	11111	101011	010100
				K.28	11100	001111	110000

不均等性的執行規則

Previous RD	Disparity of 6 or 4 Bit Code	Disparity chosen	Next RD
−1	0	0	−1
−1	±2	+2	+1
+1	0	0	+1
+1	±2	−2	−1

3b/4b code

input		RD = −1	RD = +1	input		RD = −1	RD = +1
	HGF	fghj			HGF	fghj	
D.x.0	000	1011	0100	K.x.0	000	1011	0100
D.x.1	001	1001		K.x.1 ‡	001	0110	1001
D.x.2	010	0101		K.x.2 ‡	010	1010	0101
D.x.3	011	1100	0011	K.x.3	011	1100	0011
D.x.4	100	1101	0010	K.x.4	100	1101	0010
D.x.5	101	1010		K.x.5 ‡	101	0101	1010
D.x.6	110	0110		K.x.6 ‡	110	1001	0110
D.x.P7 †	111	1110	0001				
D.x.A7 †	111	0111	1000	K.x.7 † ‡	111	0111	1000

控制碼

- 介面匯流排上的連結管理(Link Management)
- 連結層與資料交易層各自產生的封包(DLLP與TLP)，傳送的開始與結束也需要控制碼來標示

控制符號（Control symbols）

input		RD = −1	RD = +1
	HGF EDCBA	abcdei fghj	abcdei fghj
K.28.0	000 11100	001111 0100	110000 1011
K.28.1 †	001 11100	001111 1001	110000 0110
K.28.2	010 11100	001111 0101	110000 1010
K.28.3	011 11100	001111 0011	110000 1100
K.28.4	100 11100	001111 0010	110000 1101
K.28.5 †	101 11100	001111 1010	110000 0101
K.28.6	110 11100	001111 0110	110000 1001
K.28.7 ‡	111 11100	001111 1000	110000 0111
K.23.7	111 10111	111010 1000	000101 0111
K.27.7	111 11011	110110 1000	001001 0111
K.29.7	111 11101	101110 1000	010001 0111
K.30.7	111 11110	011110 1000	100001 0111

8b/10b encoding

- 應用：
  - PCI Express 1.x and 2.x
  - DisplayPort 1.x
  - Serial ATA
  - SD UHS-II
  - USB 3.0
  - Thunderbolt 1.x and 2.x
- 缺點：
  - 增加20%非實際資料傳輸

128b/130b encoding

- 應用：
  - PCI Express 3.0/4.0
  - DisplayPort 2.0
  - USB3.2 GEN2

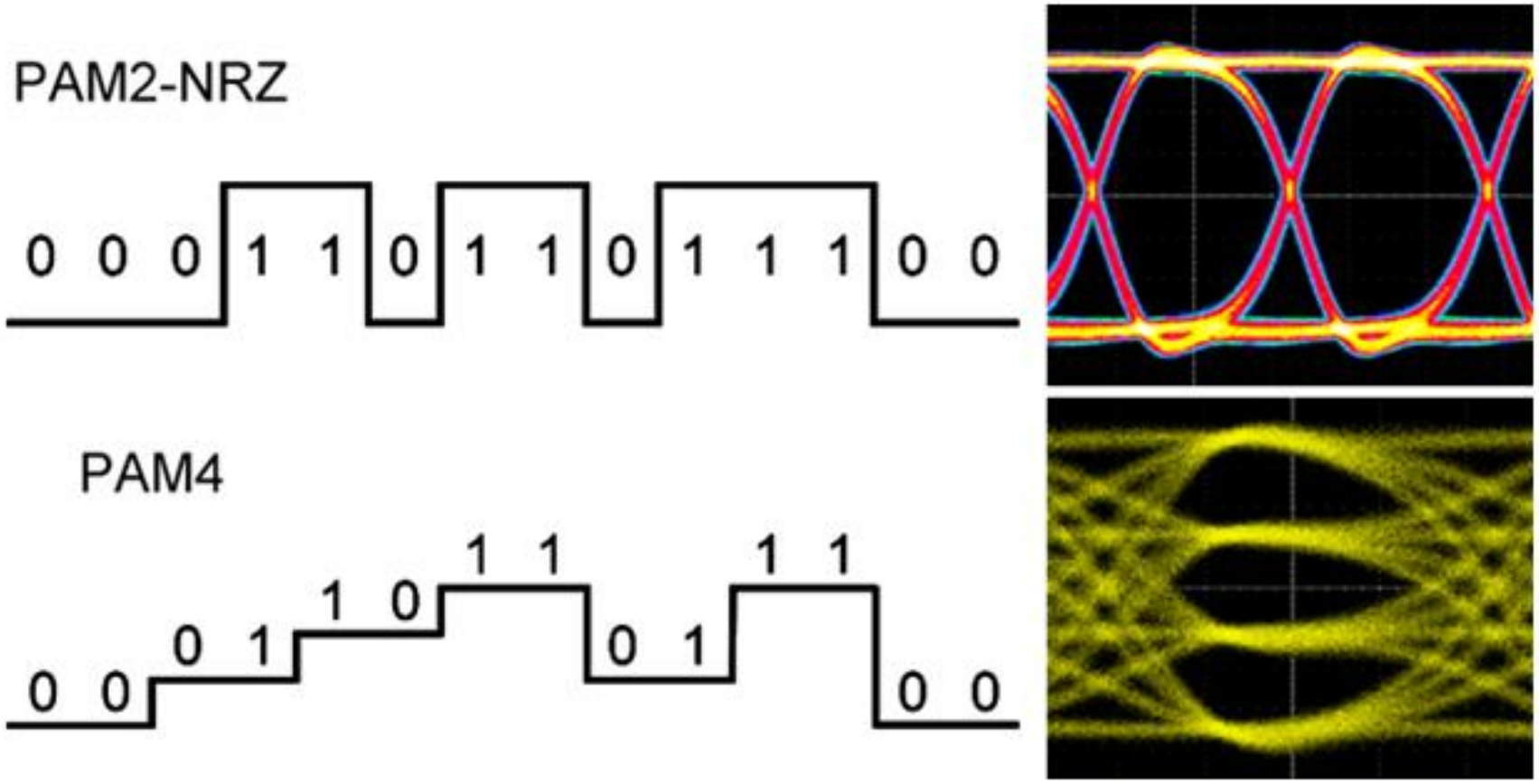
PCI-E

PCI Express link performance[47][48]

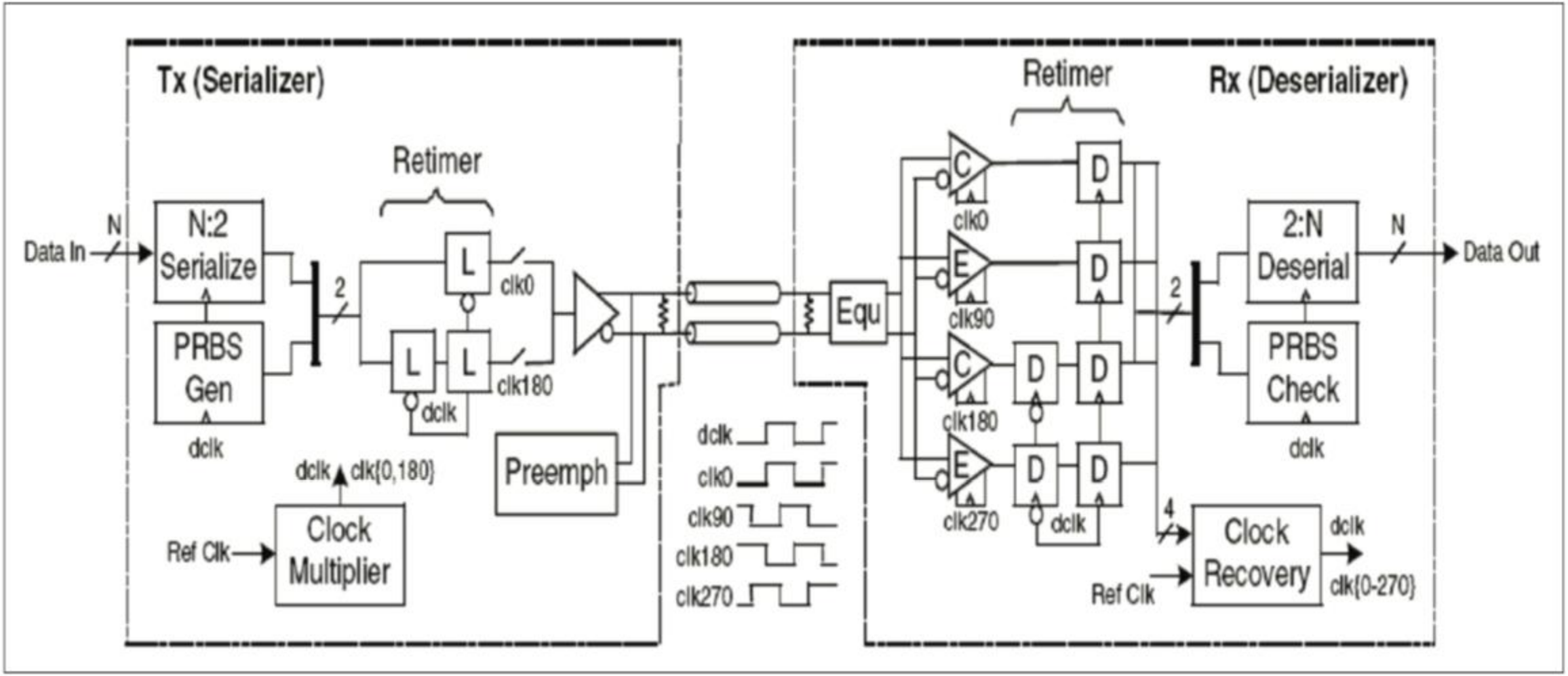
Version	Intro-duced	Line code		Transfer rate per lane[i][ii]	Throughput[i][iii]				
					x1	x2	x4	x8	x16
1.0	2003	NRZ	8b/10b	2.5 GT/s	0.250 GB/s	0.500 GB/s	1.000 GB/s	2.000 GB/s	4.000 GB/s
2.0	2007			5.0 GT/s	0.500 GB/s	1.000 GB/s	2.000 GB/s	4.000 GB/s	8.000 GB/s
3.0	2010		128b/130b	8.0 GT/s	0.985 GB/s	1.969 GB/s	3.938 GB/s	7.877 GB/s	15.754 GB/s
4.0	2017			16.0 GT/s	1.969 GB/s	3.938 GB/s	7.877 GB/s	15.754 GB/s	31.508 GB/s
5.0	2019			32.0 GT/s	3.938 GB/s	7.877 GB/s	15.754 GB/s	31.508 GB/s	63.015 GB/s
6.0	2022	PAM-4 FEC	1b/1b 242B/256B FLIT	64.0 GT/s 32.0 GBd	7.563 GB/s	15.125 GB/s	30.250 GB/s	60.500 GB/s	121.000 GB/s
7.0	2025 (planned)			128.0 GT/s 64.0 GBd	15.125 GB/s	30.250 GB/s	60.500 GB/s	121.000 GB/s	242.000 GB/s

NRZ & PAM4

Eye Diagram



SerDes電路


Tx (Serializer)
Retimer
Rx (Deserializer)
Retimer
Data In
N
N:2 Serialize
PRBS Gen
dclk
2
L
clk0
clk180
dclk
Preemph
dclk
clk{0,180}
Ref Clk
Clock Multiplier
dclk
clk0
clk90
clk180
clk270
Equ
C
E
clk0
clk90
clk180
clk270
D
2
2:N Deserial
PRBS Check
dclk
N
Data Out
4
Clock Recovery
Ref Clk
dclk
clk{0-270}

Transmitter

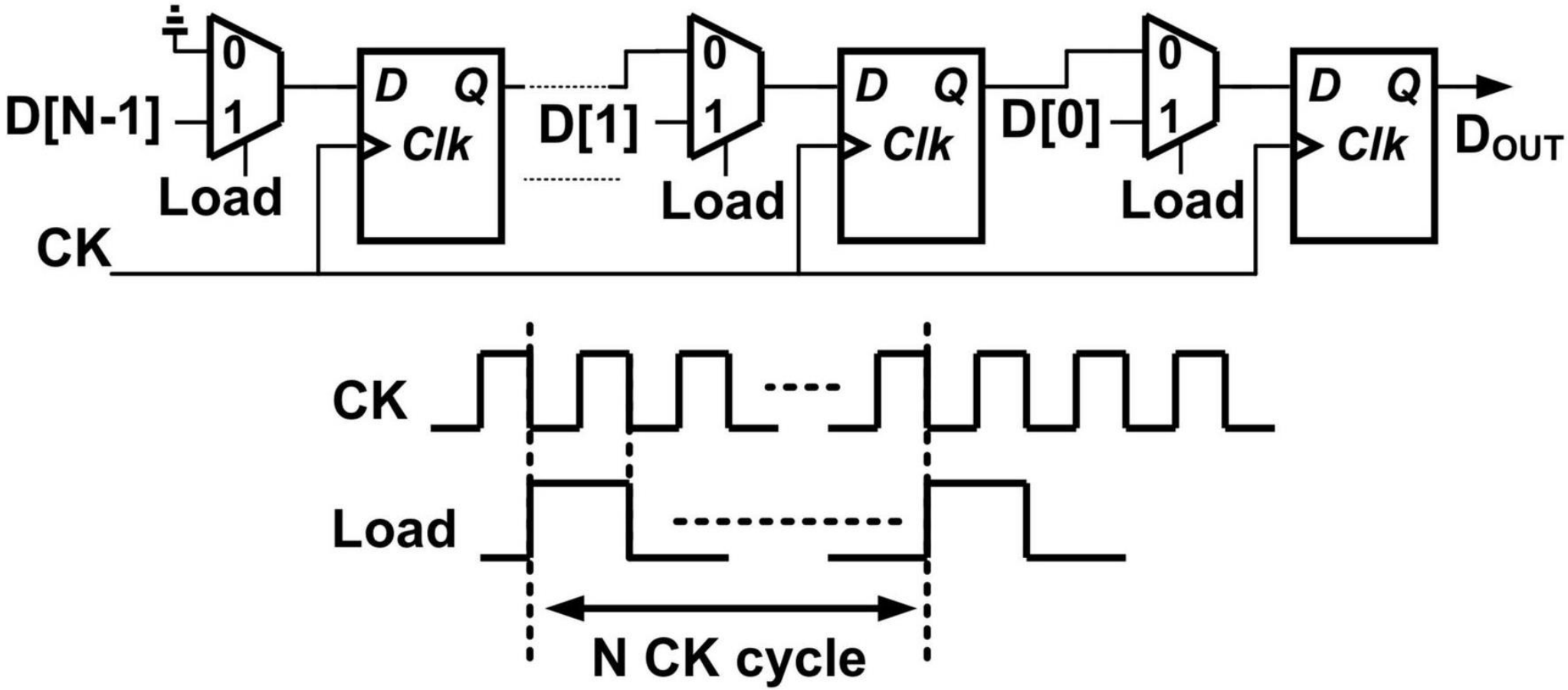
Basic Function:

Serializer: Convert parallel data to serial data

Pre-driver: Serve as a buffer for driver

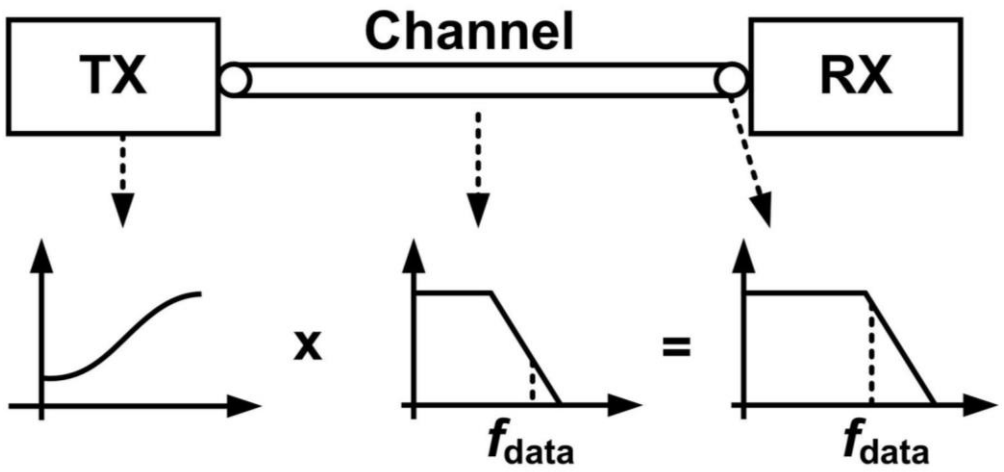
Driver: Drive output signal with 50Ω output impedance

N to 1 Serializer



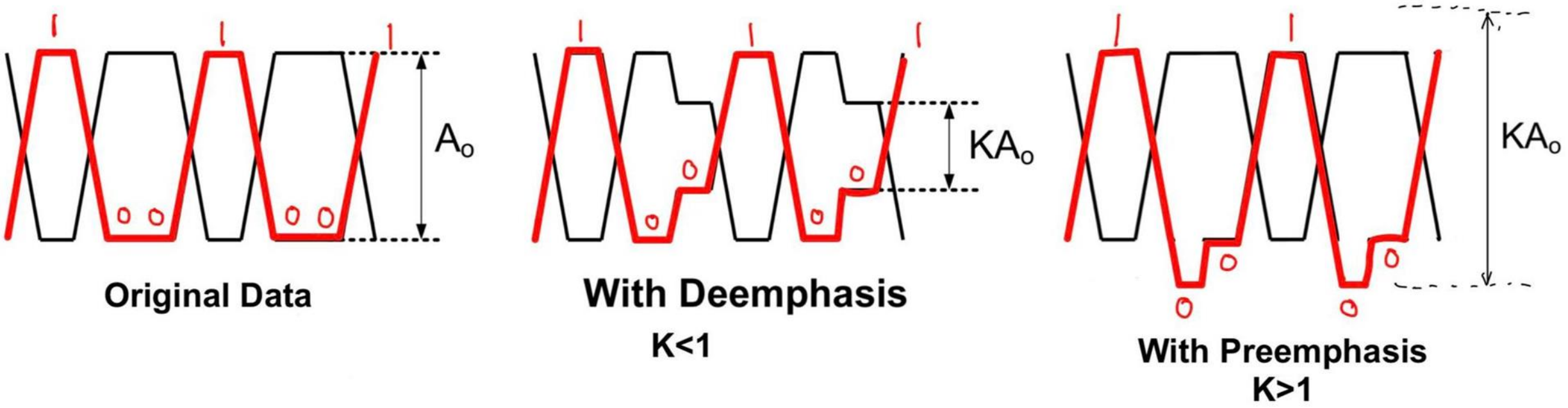
Pre-emphasis & De-emphasis

- 減少符碼間干擾(inter-symbol interference, or ISI)
- 抵銷channel loss

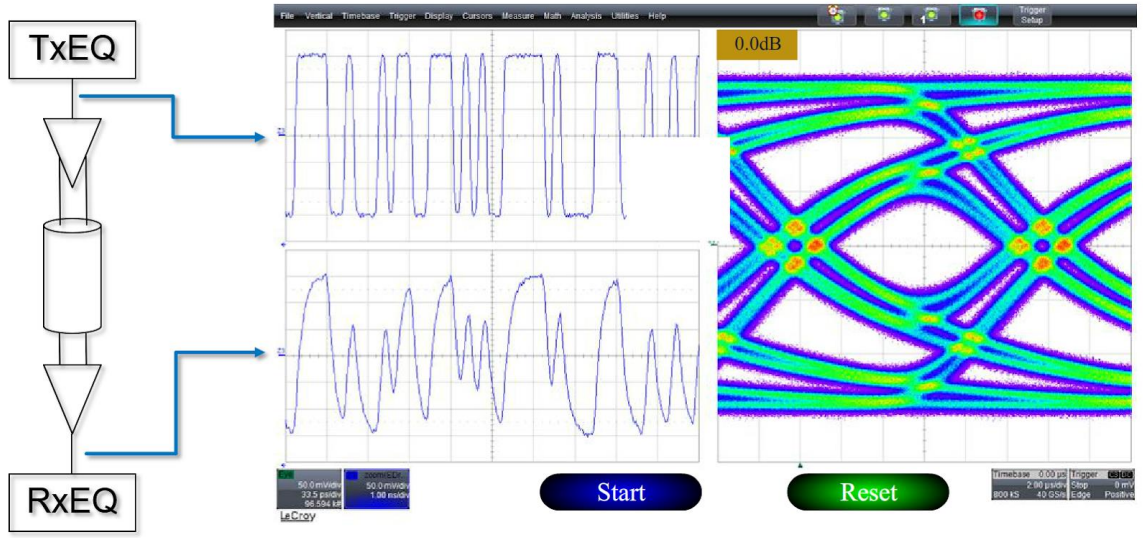


Pre-emphasis & De-emphasis

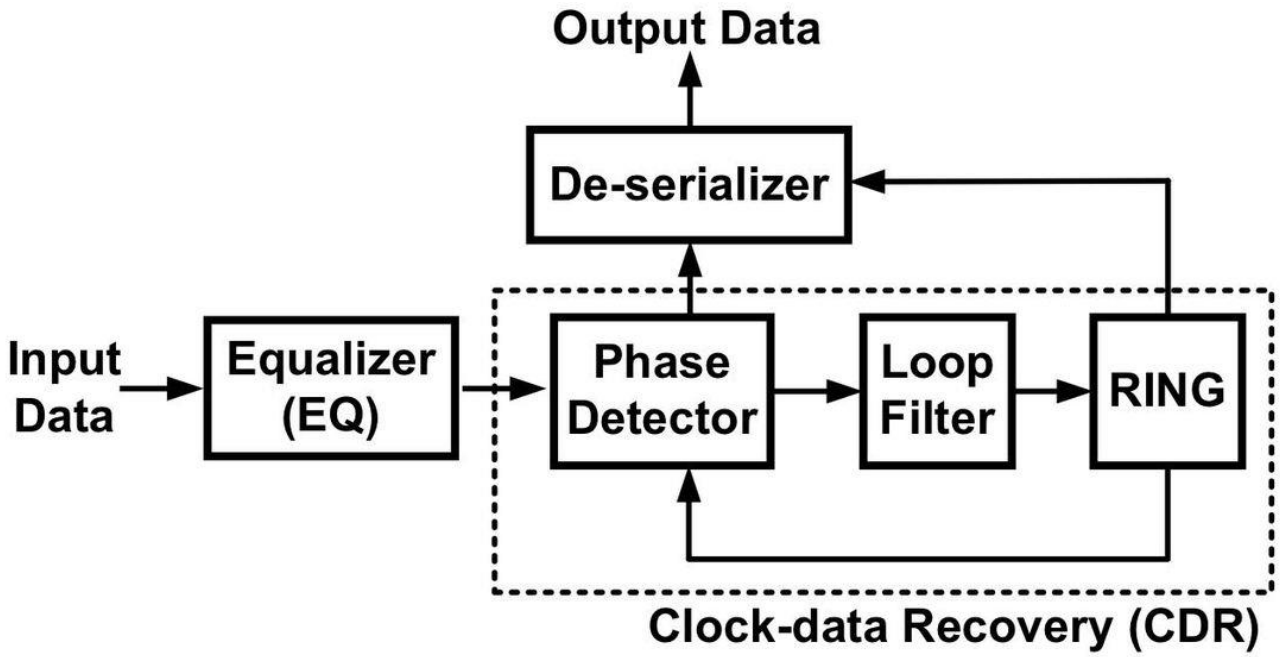
- 在Tx端進行High-pass訊號處理
  - Pre-emphasis: 增加高頻成分
  - De-emphasis: 減少低頻成分



Pre-emphasis & De-emphasis



Receiver



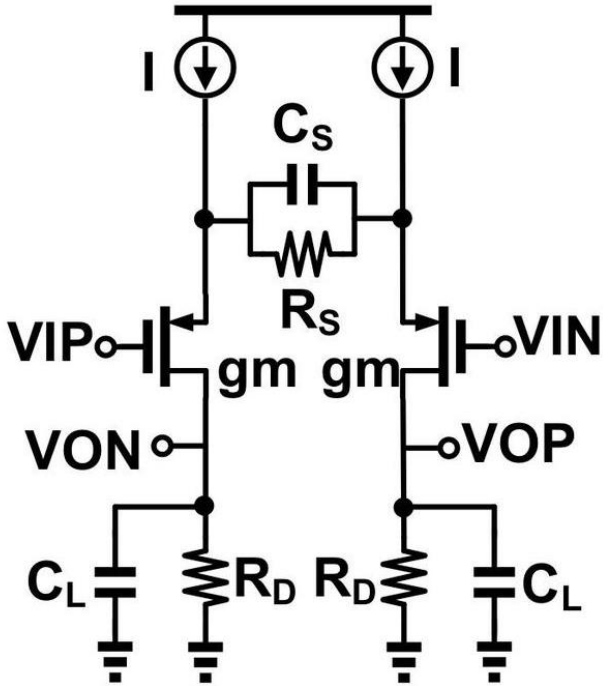
EQ: Compensate the channel loss

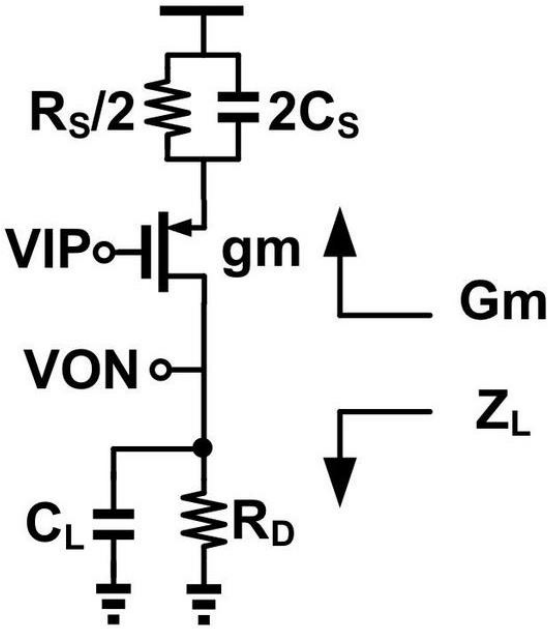
CDR: Recover clock; align CK0 with the data edge, and sample the data center by CK180 (full rate)

Deserializer:

Input serial data in high speed and output parallel data in low speed

Core of Equalizer

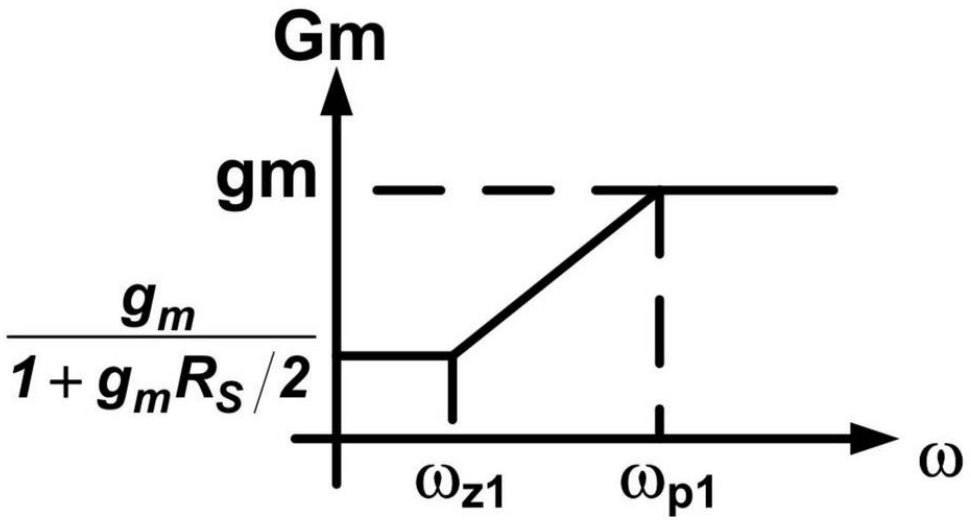


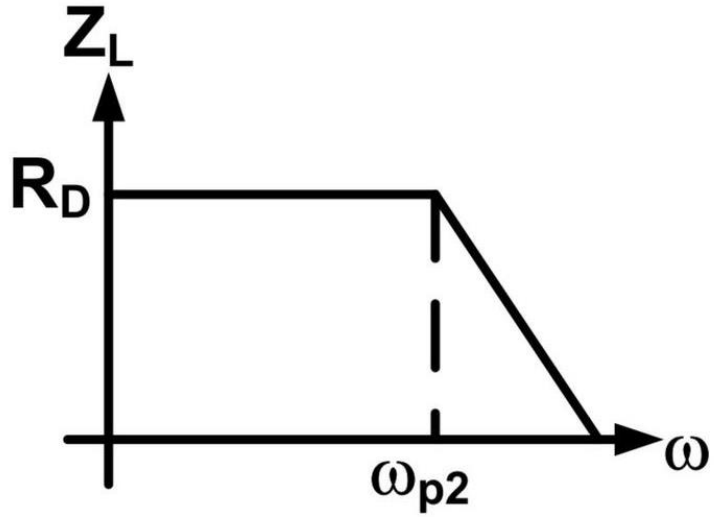


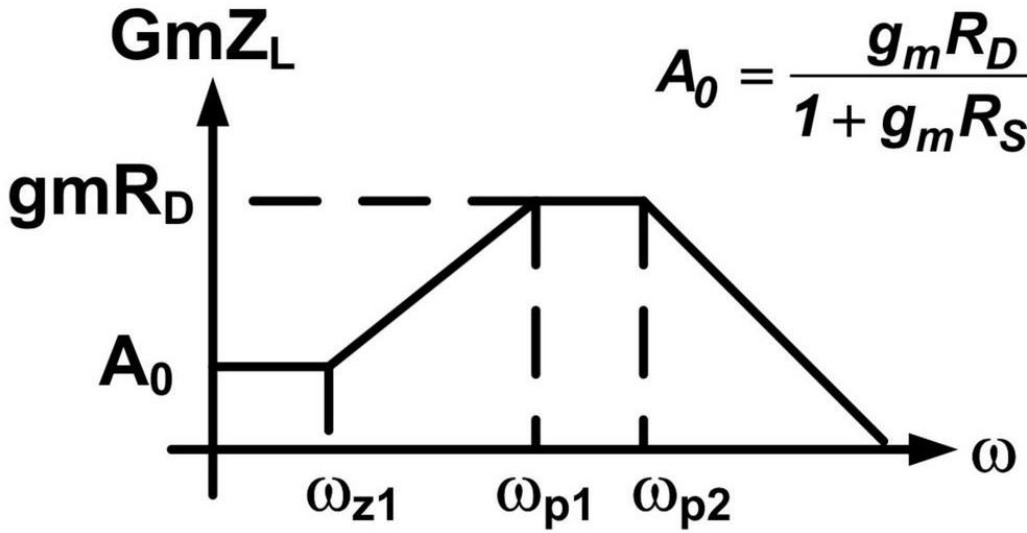
$$Gm = \frac{g_m}{1 + g_m\left(\frac{R_S}{2} \,//\, \frac{1}{2C_S s}\right)} = \frac{g_m\left(R_S C_S s + 1\right)}{R_S C_S s + 1 + g_m R_S/2}$$

$$Z_L = \frac{R_D}{1 + sR_D C_L}$$

Equalizer frequency response







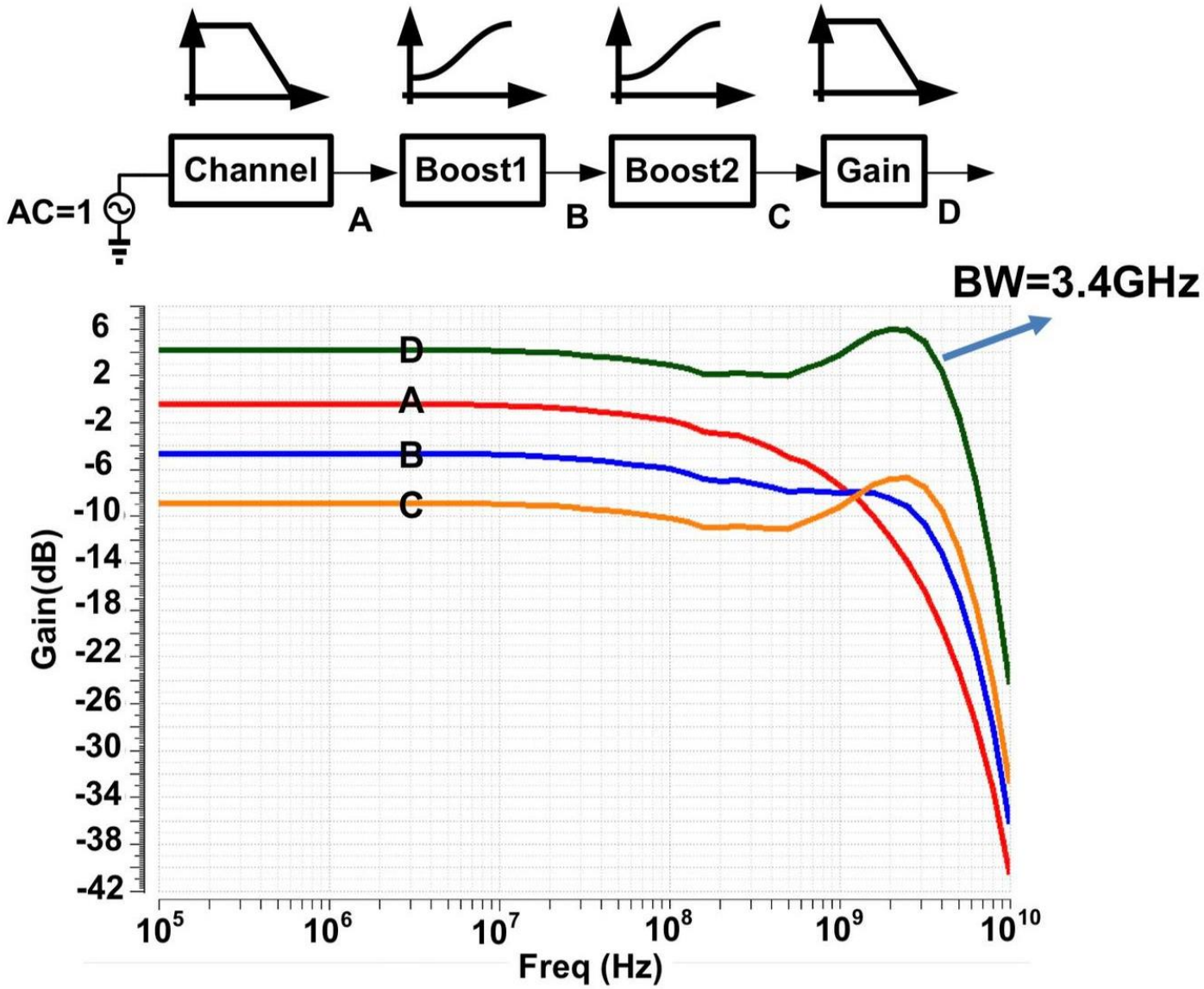
$$A_0 = \frac{g_m R_D}{1 + g_m R_S/2}$$

$$\omega_{z1} = \frac{1}{R_S C_S}$$

$$\omega_{p1} = \frac{1 + g_m R_S/2}{R_S C_S}$$

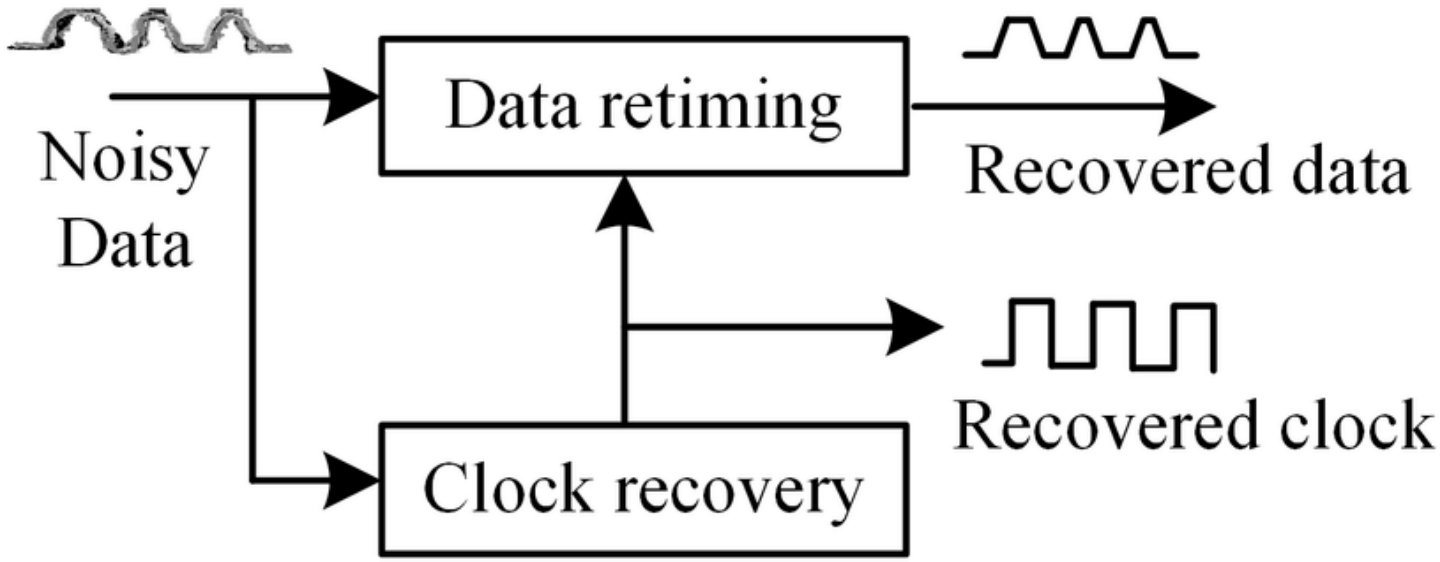
$$\omega_{p2} = \frac{1}{R_D C_L}$$

Compensation of channel loss

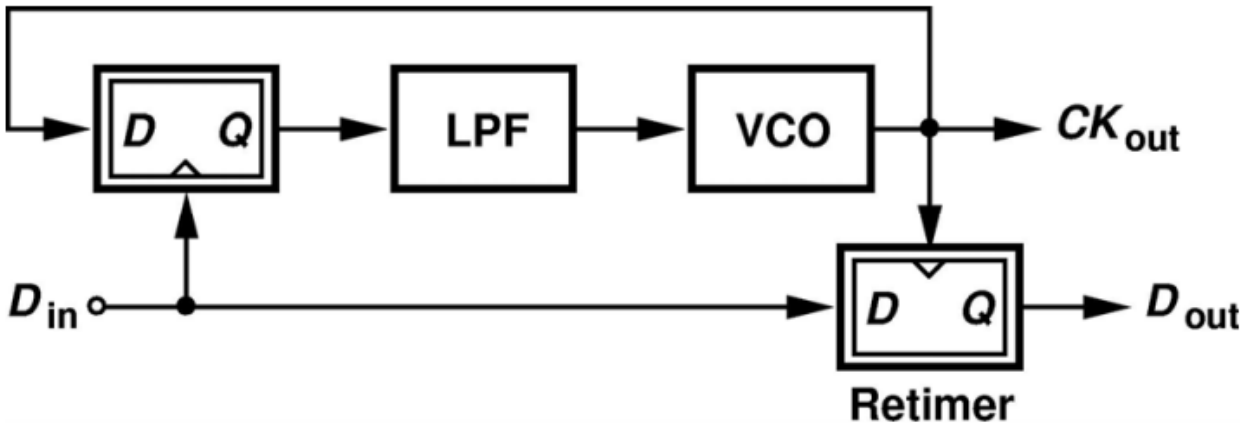


Clock Data Recovery

- CDR
- 從資料中找出clock訊號
- 用clock還原出乾淨的數位訊號

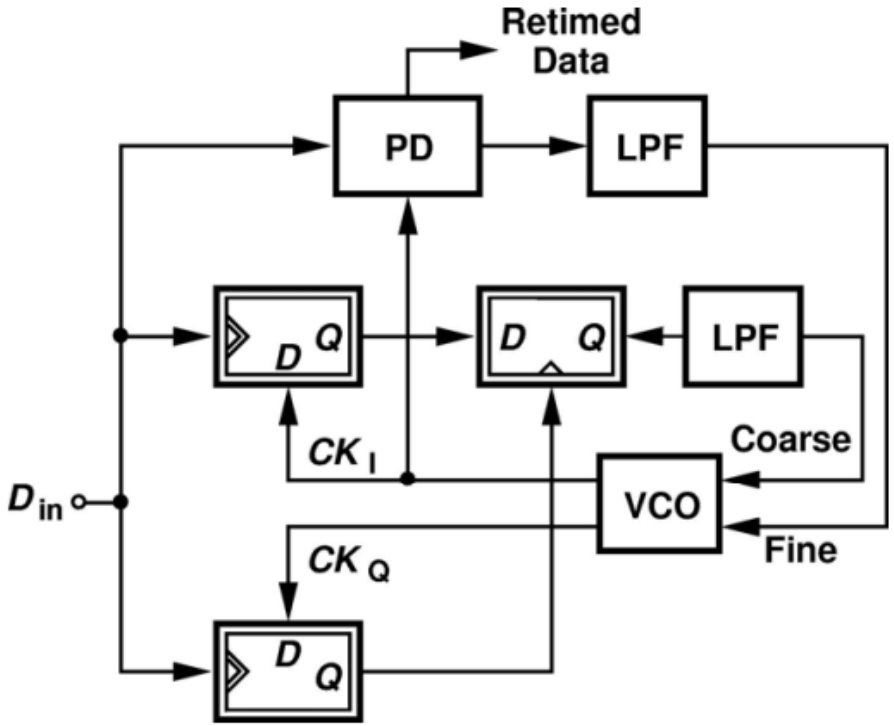


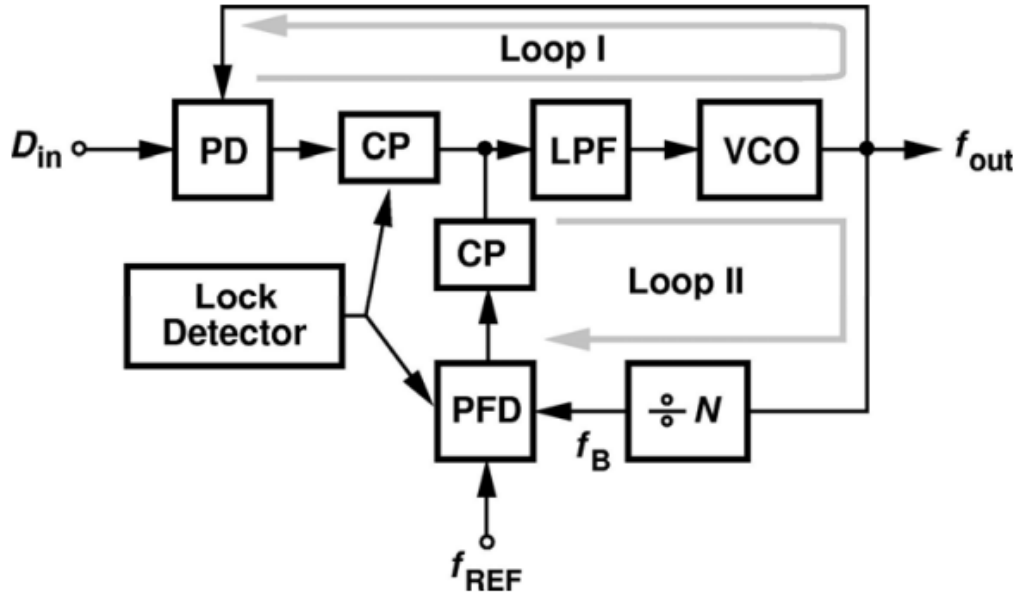
Simple CDR Architecture



- Drawbacks:
  - Continue to increase or decrease the VCO control voltage even when no data edge is present ⇒ large jitter.
  - Large skews may cause improper sampling.
  - Finite capture range (lack of frequency acquisition loop).

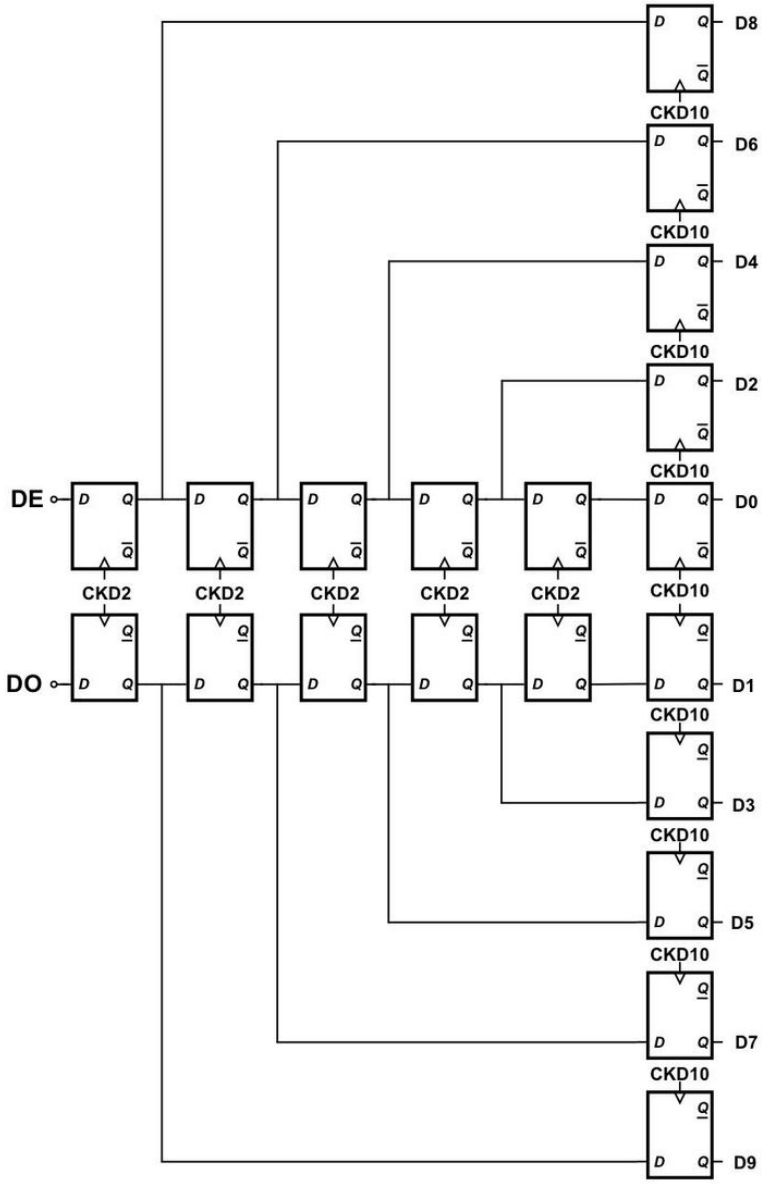
Alternative CDR Architecture





- FD loop pushes the oscillation frequency to roughly-right position.
- PD loop then takes over to lock the phase.
- Lock detector is required to shut down the FD upon lock.

Deserializer

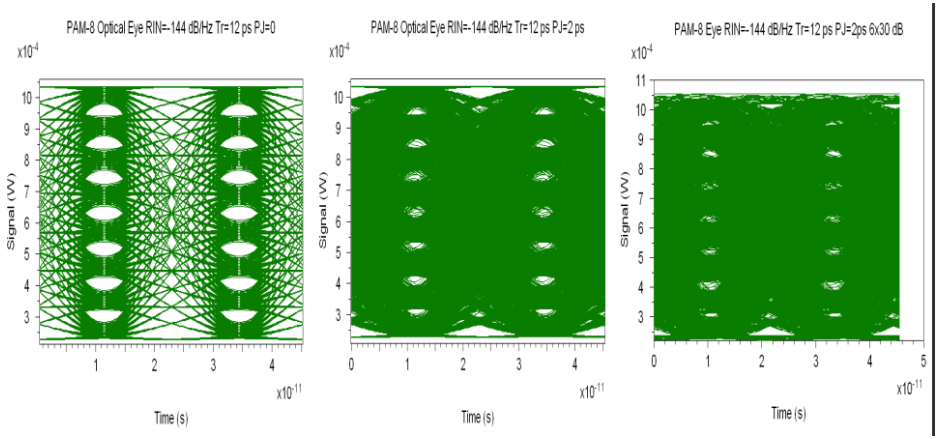


Clock 0°
Clock 180°

總結

- SerDes:

- 運用一些技巧來抵銷高速傳輸下的channel loss:
  - Line coding: 8b/10b, 128b/130b
  - Pre-emphasis/De-demphasis
  - Equalizer
- 未來:
  - PAM 4/6/8?



Reference

- Wikipedia_8b/10b encoding
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Thank you for listening